

## Refine Search

### Search Results -

Term	Documents
(9 AND 24).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	30
(L24 AND L9).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	30

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L28





### Search History

DATE: Friday, November 16, 2007

[Purge Queries](#)[Printable Copy](#)[Create Case](#)

Set  
Name   Query

side by  
 side

Hit   Set  
Count   Name  
 result set

*DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*

L28   L24 and I9

30   L28

L27   L24 and I8

10   L27

L26   L24 and I7

55   L26

<u>L25</u>	L24 and I6	73	<u>L25</u>
<u>L24</u>	address\$5 near5 (translat\$6 or convert\$4 or conversion\$1) and I19	80	<u>L24</u>
<u>L23</u>	L19 and I9	43	<u>L23</u>
<u>L22</u>	L19 and I8	14	<u>L22</u>
<u>L21</u>	L19 and I7	114	<u>L21</u>
<u>L20</u>	L19 and I6	140	<u>L20</u>
<u>L19</u>	L18 and address\$4 near5 (tbt or tlb or table)	157	<u>L19</u>
<u>L18</u>	taken and I2	260	<u>L18</u>

*DB=PGPB,USPT; PLUR=YES; OP=OR*

<u>L17</u>	I4 and I9	76	<u>L17</u>
<u>L16</u>	I4 and I8	11	<u>L16</u>
<u>L15</u>	I4 and I7	84	<u>L15</u>
<u>L14</u>	I4 and I6	139	<u>L14</u>
<u>L13</u>	I3 and I9	99	<u>L13</u>
<u>L12</u>	I3 and I8	16	<u>L12</u>
<u>L11</u>	I3 and I7	174	<u>L11</u>
<u>L10</u>	I3 and I6	246	<u>L10</u>
<u>L9</u>	(712/201-219)![CCLS]	4716	<u>L9</u>
<u>L8</u>	(711/201-221)[CCLS]	7018	<u>L8</u>
<u>L7</u>	(712/225-242)[CCLS]	4791	<u>L7</u>
<u>L6</u>	(712/2-300)[CCLS]	13900	<u>L6</u>

*DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*

<u>L5</u>	L4 and descriptor\$1	26	<u>L5</u>
<u>L4</u>	L3 and address\$5 near5 (translat\$6 or convert\$4 or conversion\$1)	148	<u>L4</u>
<u>L3</u>	L2 and (prefetch\$5 or fetch\$5)	265	<u>L3</u>
<u>L2</u>	L1 and (tbt or tlb or table) near10 (way\$1 or direct\$4 or path\$1 or target\$3)	265	<u>L2</u>
<u>L1</u>	(branch\$4) near10 (id\$1 or identif\$7) and branch\$3 near1 target near5 predict\$5	489	<u>L1</u>

END OF SEARCH HISTORY



Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "((predict\* and table and address and branch\*)&lt;in&gt;metadata)"

Your search matched 16 of 1687657 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.



» Search Options

[View Session History](#)[New Search](#)

» Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

Modify Search


☐ Check to search only within this results set

 Display Format: ☒ Citation ☐ Citation & Abstract

IEEE/IET

Books

Educational Courses

IEEE/IET Journals, transactions, letters, magazines, conference proceedings, and standards.

 

- |                          |   |
|--------------------------|---|
| <input type="checkbox"/> | <b>1. Branch predictor prediction: a power-aware branch predictor for high-performance proces:</b><br>Baniasadi, A.; Moshovos, A.;<br><u>Computer Design: VLSI in Computers and Processors, 2002. Proceedings. 2002 IEEE Internation</u><br>16-18 Sept. 2002 Page(s):458 - 461<br>Digital Object Identifier 10.1109/ICCD.2002.1106813<br><u>AbstractPlus</u>   Full Text: <u>PDF</u> (341 KB) IEEE CNF<br><u>Rights and Permissions</u>         |
| <input type="checkbox"/> | <b>2. Design optimization for high-speed per-address two-level branch predictors</b><br>Chen, I.-C.K.; Chih-Chieh Lee; Postiff, M.; Mudge, T.;<br><u>Computer Design: VLSI in Computers and Processors, 1997. ICCD '97. Proceedings., 1997 IEEE</u><br>12-15 Oct. 1997 Page(s):88 - 96<br>Digital Object Identifier 10.1109/ICCD.1997.628854<br><u>AbstractPlus</u>   Full Text: <u>PDF</u> (1108 KB) IEEE CNF<br><u>Rights and Permissions</u> |
| <input type="checkbox"/> | <b>3. Accurate indirect branch prediction</b><br>Driesen, K.; Holzle, U.;<br><u>Computer Architecture, 1998. Proceedings. The 25th Annual International Symposium on</u><br>27 June-1 July 1998 Page(s):167 - 178<br>Digital Object Identifier 10.1109/ISCA.1998.694772<br><u>AbstractPlus</u>   Full Text: <u>PDF</u> (108 KB) IEEE CNF<br><u>Rights and Permissions</u>   |
| <input type="checkbox"/> | <b>4. Exploring design space of scalable per-address branch predictors</b><br>Kongmunvattana, A.; Tiamkaew, E.;<br><u>TENCON 2004. 2004 IEEE Region 10 Conference</u><br>Volume B, 21-24 Nov. 2004 Page(s):156 - 159 Vol. 2<br>Digital Object Identifier 10.1109/TENCON.2004.1414555<br><u>AbstractPlus</u>   Full Text: <u>PDF</u> (1848 KB) IEEE CNF<br><u>Rights and Permissions</u>   |
| <input type="checkbox"/> | <b>5. The effects of mispredicted-path execution on branch prediction structures</b>  |

Jourdan, S.; Tse-Hao Hsing; Stark, J.; Patt, Y.N.;  
[Parallel Architectures and Compilation Techniques, 1996... Proceedings of the 1996 Conference.c](#)  
20-23 Oct. 1996 Page(s):58 - 67  
Digital Object Identifier 10.1109/PACT.1996.552555  
[AbstractPlus](#) | [Full Text: PDF\(964 KB\)](#) IEEE CNF  
[Rights and Permissions](#)

- ☐ 6. **Evaluating branch prediction using two-level perceptron table**  
Ribas, L.V.M.; Goncalves, R.A.L.;  
[Parallel, Distributed, and Network-Based Processing, 2006. PDP 2006. 14th Euromicro Internatio](#)  
15-17 Feb. 2006 Page(s):4 pp.  
Digital Object Identifier 10.1109/PDP.2006.34  
[AbstractPlus](#) | [Full Text: PDF\(152 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 7. **Branch history table indexing to prevent pipeline bubbles in wide-issue superscalar proces**  
Tse-Yu Yeh; Patt, Y.N.;  
[Microarchitecture, 1993. Proceedings of the 26th Annual International Symposium on](#)  
1-3 Dec. 1993 Page(s):164 - 175  
Digital Object Identifier 10.1109/MICRO.1993.282746  
[AbstractPlus](#) | [Full Text: PDF\(972 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 8. **Microarchitecture support for reducing branch penalty in a superscaler processor**  
Sakamoto, M.; Nunomura, Y.; Yoshida, T.; Shimazu, Y.;  
[Computer Design: VLSI in Computers and Processors, 1996. ICCD '96. Proceedings., 1996 IEEE](#)  
7-9 Oct. 1996 Page(s):208 - 216  
Digital Object Identifier 10.1109/ICCD.1996.563559  
[AbstractPlus](#) | [Full Text: PDF\(776 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 9. **Influence of high-level program structures on branch prediction accuracy**  
Ganjoo, A.; Nian-Feng Tzeng;  
[Euromicro Conference, 2000. Proceedings of the 26th](#)  
Volume 1, 5-7 Sept. 2000 Page(s):316 - 322 vol.1  
Digital Object Identifier 10.1109/EURMIC.2000.874648  
[AbstractPlus](#) | [Full Text: PDF\(540 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 10. **DStride: data-cache miss-address-based stride prefetching scheme for multimedia proces**  
Hariprakash, G.; Achutharaman, R.; Omondi, A.R.;  
[Computer Systems Architecture Conference, 2001. ACSAC 2001. Proceedings. 6th Australasian](#)  
29-30 Jan. 2001 Page(s):62 - 70  
Digital Object Identifier 10.1109/ACAC.2001.903360  
[AbstractPlus](#) | [Full Text: PDF\(756 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 11. **Branch prediction and simultaneous multithreading**  
Hily, S.; Seznec, A.;  
[Parallel Architectures and Compilation Techniques, 1996... Proceedings of the 1996 Conference.c](#)  
20-23 Oct. 1996 Page(s):169 - 173  
Digital Object Identifier 10.1109/PACT.1996.552664  
[AbstractPlus](#) | [Full Text: PDF\(556 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ 12. **TCP: tag correlating prefetchers**  
Hu, Z.; Martonosi, M.; Kaxiras, S.;  
[High-Performance Computer Architecture, 2003. HPCA-9 2003. Proceedings. The Ninth Internati](#)  
8-12 Feb. 2003 Page(s):317 - 326

Digital Object Identifier 10.1109/HPCA.2003.1183549

[AbstractPlus](#) | [Full Text: PDF\(348 KB\)](#) | [IEEE CNF](#)  
[Rights and Permissions](#)



**13. Augmenting Branch Predictor to Secure Program Execution**

Shi, Yixin; Lee, Gyungho;

[Dependable Systems and Networks, 2007. DSN '07. 37th Annual IEEE/IFIP International Conference on](#)  
25-28 June 2007 Page(s):10 - 19

Digital Object Identifier 10.1109/DSN.2007.19

[AbstractPlus](#) | [Full Text: PDF\(377 KB\)](#) | [IEEE CNF](#)  
[Rights and Permissions](#)



**14. Architectural Support for Run-Time Validation of Control Flow Transfer**

Shi, Yixin; Dempsey, Sean; Lee, Gyungho;

[Computer Design, 2006. ICCD 2006. International Conference on](#)  
1-4 Oct. 2007 Page(s):506 - 513

Digital Object Identifier 10.1109/ICCD.2006.4380863

[AbstractPlus](#) | [Full Text: PDF\(416 KB\)](#) | [IEEE CNF](#)  
[Rights and Permissions](#)



**15. An X86 microprocessor with multimedia extensions**

Draper, D.A.; Crowley, M.P.; Holst, J.; Favor, G.; Schoy, A.; Ben-Meir, A.; Trull, J.; Khanna, R.; W  
Partovi, H.; Johnson, M.; Lee, T.; Mallick, D.; Frydel, G.; Vuong, A.; Yu, S.; Maley, R.; Kauffmann,  
[Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC., 1997. IEEE Inter](#)  
6-8 Feb. 1997 Page(s):172 - 173, 450

Digital Object Identifier 10.1109/ISSCC.1997.585321

[AbstractPlus](#) | [Full Text: PDF\(872 KB\)](#) | [IEEE CNF](#)  
[Rights and Permissions](#)



**16. Instruction cache prefetching with extended BTB**

Shuh-An Chi; R-Ming Shiu; Jih-Chang Chiu; Si-En Chang; Chung-Ping Chung;

[Parallel and Distributed Systems, 1997. Proceedings., 1997 International Conference on](#)  
10-13 Dec. 1997 Page(s):360 - 365

Digital Object Identifier 10.1109/CPADS.1997.652574

[AbstractPlus](#) | [Full Text: PDF\(564 KB\)](#) | [IEEE CNF](#)  
[Rights and Permissions](#)

[Help](#) [Contact](#)

[© Copy](#)

Indexed by  
 Inspec<sup>®</sup>